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US005875198A

United States Patent [19]

Satoh

[11] Patent Number: 5,875,198

[45] Date of Patent: Feb. 23, 1999

[54] **SEMICONDUCTOR DEVICE TESTING APPARATUS**

[75] Inventor: Kazuhiko Satoh, Gyoda, Japan

[73] Assignee: Advantest Corporation, Tokyo, Japan

[21] Appl. No.: 907,368

[22] Filed: Aug. 7, 1997

[30] Foreign Application Priority Data

Aug. 8, 1996 [JP] Japan 8-210068

[51] Int. Cl.[6] G01R 31/28; G06F 11/00

[52] U.S. Cl. 371/27.3; 371/22.1; 371/27.1

[58] Field of Search 371/27.3, 27.1, 371/22.1

[56] References Cited

U.S. PATENT DOCUMENTS

5,748,134 5/1998 Rowshtal et al. 341/120

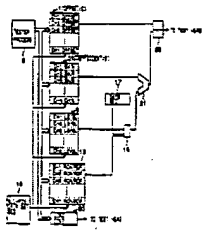
Primary Examiner—Phung M. Chung

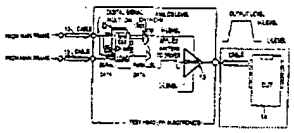
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

A semiconductor device testing apparatus is provided which includes an output voltage corrective circuit wherein a test voltage to be applied to a semiconductor under test (DUT) 14 is corrected through digital processing. An offset memory 1, a gain memory 2, an output level register 3, a timer processor 8, a selector register 18, a selector 16, a data register 17, an all-pin data setting sequencer 19, a load controller 20, a digital multiplier 21, and a digital adder 22 are provided in the main frame of the testing apparatus. A multi-channel D/A converter 23 for converting digital serial data from the main frame to analog parallel data for each channel and drivers 13 each for applying the test voltage to one of the pins of the DUT 14 are provided in the test head of the testing apparatus. The offset memory 1 prestores therein offset data contained in correction data and the gain memory gain data also contained in the correction data. The output level register 3 stores therein the test voltage to be applied to the pin of the DUT for each channel.

10 Claims, 12 Drawing Sheets





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US-PAT-NO: 5875198

DOCUMENT-IDENTIFIER: US 5875198 A

TITLE: Semiconductor device testing apparatus

Brief Summary Text - BSTX (43):

In a first aspect of the present invention, there is provided a semiconductor device testing apparatus comprising: an output level register for storing therein the voltage of a voltage signal per channel to be applied to a semiconductor device to be tested; a correction data memory for previously storing therein correction data per channel which is used to correct variations of each channel so that the voltage of a voltage signal to be applied to a semiconductor device under test comes to equal to the voltage of the voltage signal from the output level register; digital operation means for processing the voltage of the voltage signal per channel from the output level register and the correction data per channel from the correction data memory through digital operation and outputting the result of the digital operation as a corrected voltage of the voltage signal per channel to a corresponding channel; a multi-channel digital-to-analog converter for converting a serial digital voltages transmitted thereto via a first signal transmission means from the digital operation means into parallel analog voltages corresponding to each channel; a load controller for supplying via a second signal transmission means to the multi-channel digital-to-analog converter a load control signal for controlling the timing when the parallel analog voltages are outputted from the multi-channel digital-to-analog converter; and driver means for applying the parallel analog voltages from the multi-channel digital-to-analog converters to a semiconductor device under test, the number of the driver means being equal to that of the channels used.

Claims Text - CLTX (5):

a multi-channel digital-to-analog converter for converting a serial digital voltages transmitted thereto via a first signal transmission means from said digital operation means into parallel analog voltages corresponding to each channel;

Current US Original Classification - CCOR (1):

Details | Text | Image | HTML | KWIC

14	☐	☐	US 5295080 A	19940315	7	Method of operating a buffer memory to provide a trigger 714/
15	☐	☑	US 4751670 A	19880614	11	High integrity digital processor architecture 701/
16	☐	☑	US 4658209 A	19870414	9	Universal test board, serial input (for synthesizer 714/
17	☑	☐	US 4646303 A	19870224	20	Data error detection and 714/

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US 20020145437A1

(19) **United States**

(12) **Patent Application Publication** (10) Pub. No.: US 2002/0145437 A1

Sporck et al. (43) Pub. Date: Oct. 10, 2002

(54) **PROBE CARD WITH COPLANAR DAUGHTER CARD**

(75) Inventors: A. Nicholas Sporck, Saratoga, CA (US); Makarand S. Shinde, Dublin, CA (US)

Correspondence Address:
FORMFACTOR, INC.
LEGAL DEPARTMENT
2140 RESEARCH DRIVE
LIVERMORE, CA 94550 (US)

(73) Assignee: FormFactor, Inc.

(21) Appl. No.: 09/812,913

(22) Filed: Apr. 10, 2001

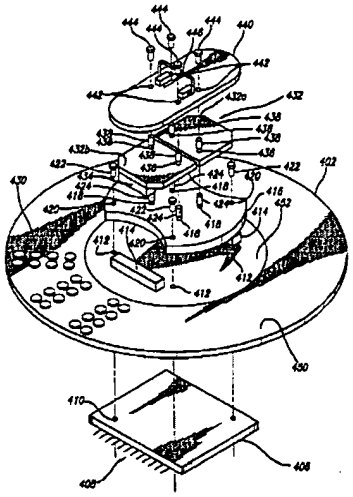
Publication Classification

(51) Int. Cl.[7] G01R 31/02

(52) U.S. Cl. 324/754

(57) **ABSTRACT**

A probe card assembly includes a printed circuit board with tester contacts for making electrical connections to a semiconductor tester. The probe card assembly also includes a probe head assembly with probes for contacting a semiconductor device under test. One or more daughter cards is mounted to the printed circuit board such that they are substantially coplanar with the printed circuit board. The daughter cards may contain a circuit for processing test data, including test signals to be input into the semiconductor and/or response signals generated by the semiconductor device in response to the test signals.



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DOCUMENT-IDENTIFIER: US 20020145437 A1

TITLE: Probe card with coplanar daughter card

Pre-Grant Publication Document Identifier - DID (1):

US 20020145437 A1

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8	☐	☑	US 4751670 A	19880614	11	High integrity digital processor architecture	701/
9	☐	☑	US 4658209 A	19870414	9	Universal test board, serial input (for synthesizer	714/
10	☐	☑	US 4055801 A	19771025	20	Automatic electronic test equipment and method	714/
11	☐	☑	US 4001559 A	19770104	22	Programmable measuring	714/

Details Text Image HTML

US 20020105352A1

(19) **United States**

(12) **Patent Application Publication** (10) Pub. No.: US 2002/0105352 A1

Mori et al. (43) Pub. Date: Aug. 8, 2002

(54) APPARATUS AND METHOD FOR TESTING SEMICONDUCTOR INTEGRATED CIRCUIT

(75) Inventors: Hisaya Mori, Hyogo (JP); Shinji Yamada, Hyogo (JP); Tsuyhiko Furukura, Tokyo (JP)

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600 13th Street, N.W.
Washington, DC 20005-3096 (US)

(73) Assignee: MITSUBISHI DENKI KABUSHIKI KAISHA

(21) Appl. No.: 09/927,368

(22) Filed: Aug. 13, 2001

(30) Foreign Application Priority Data

Feb. 8, 2001 (JP) 2001-032596

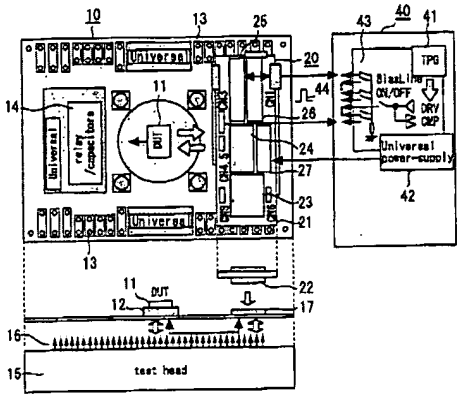
Publication Classification

(51) Int. Cl.[7] G01R 31/26

(52) U.S. Cl. 324/765

(57) ABSTRACT

A test ancillary device with data memory and an analysis section is disposed in the vicinity of a test circuit board. The data memory is divided into two memory sections such that, when digital test data are stored in one memory section, the digital test data that have already been stored in the other memory section are loaded for analysis purpose.



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DOCUMENT-IDENTIFIER: US 20020105352 A1

TITLE: Apparatus and method for testing semiconductor integrated circuit

Pre-Grant Publication (PGPub) Document Number - PGNR (1):

20020105352

Summary of Invention Paragraph - BSTX (3):

[0002] The present invention relates to an apparatus for testing a semiconductor integrated circuit. More particularly the present invention relates to an apparatus for testing a semiconductor integrated circuit including an analog-to-digital converter circuit for converting an analog signal into a digital signal or a digital-to-analog converter circuit for converting a digital signal into an analog signal, as well as to a method of testing a semiconductor integrated circuit using the apparatus.

Summary of Invention Paragraph - BSTX (7):

[0006] A big problem with such a test apparatus lies in a test for a digital-to-analog converter circuit (DAC) for converting a digital signal into an analog signal as well as in a test for an analog-to-digital converter circuit (ADC) for converting an analog signal into a digital signal. In association with an increase in the precision of the characteristic test, embodiment of a low-cost test apparatus compatible with a semiconductor integrated circuit including the DAC and ADC has posed a challenge.

Summary of Invention Paragraph - BSTX (12):

[0010] The present invention provides an apparatus for testing a semiconductor integrated circuit which includes an analog-to-digital converter circuit or a digital-to-analog converter circuit.

Summary of Invention Paragraph - BSTX (13):

[0011] According to one aspect of the present invention, the apparatus

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L13: (21) 10 and "714"... | US 4658209 | Tag: S,P,T1 | Doc: 16/21 | "Full" 1/9 (Total...

United States Patent [19]

Page

[11] Patent Number: 4,658,209

[45] Date of Patent: Apr. 14, 1987

[54] UNIVERSAL TEST BOARD, SERIAL INPUT (FOR SYNTHESIZER TESTING)

[76] Inventor: Robert E. Page, 1945 Willow Ln., San Diego, Calif. 92106

[21] Appl. No.: 875,106

[22] Filed: Jun. 30, 1986

[51] Int. Cl.[4] G01R 31/00; G01R 31/28; G06F 11/00

[52] U.S. Cl. ..... 324/73 R; 371/17

[58] Field of Search ..... 324/73 R, 73 AT; 371/16, 27, 17, 25, 21; 370/13

[56] References Cited

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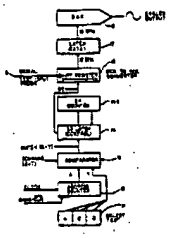
3,921,109 1/1975 Jones ..... 324/73 R
3,815,413 6/1974 Hobey 371/16
3,688,263 8/1972 Balogh, Jr. et al. 371/16
3,790,883 2/1974 James ..... 324/73 R
3,813,531 5/1974 King et al. 317/71
4,524,292 6/1985 Davis et al. 371/21
4,583,313 5/1983 Reed 370/13

Primary Examiner—Ernest F. Karlsen

[57] ABSTRACT

An electronic system that processes or otherwise acts upon a serial data stream can be monitored at any one of several points to provide an indication that specific parts as well as the whole system are functioning properly. A selected digital address is dialed on a thumbwheel switch that provides a signal indicative of a particular time slot within a repetitive sequence of time slots and a counter produces a series of digital addresses that are representative of a repetitive sequence of time slots to enable a comparison and generation of a latch signal at the particular time slot indicated. A probe is placed in electrical engagement with that portion of the signal corresponding to the selected digital address and a series test input signal is drawn from the system. The serial test input signal is converted from serial form to parallel form and a digital to analog converter generates a representative analog output signal that may be compared with a standardized analog signal that should be present at the desired point in the system when all components are functioning properly. Various synchronizing and clock signal rates can be provided to give the test apparatus the capability for accommodating differently sized signals for generating in different test analog signals.

7 Claims, 5 Drawing Figures



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L13: (21) 10 and "714"... | US 4658209 A | Tag: S,P,T1 | Doc: 16/21 | Format: KWIC

US-PAT-NO: 4658209

DOCUMENT-IDENTIFIER: US 4658209 A

TITLE: Universal test board, serial input (for synthesizer testing)

Abstract Text - ABTX (1):

An electronic system that processes or otherwise acts upon a serial data stream can be monitored at any one of several points to provide an indication that specific parts as well as the whole system are functioning properly. A selected digital address is dialed on a thumbwheel switch that provides a signal indicative of a particular time slot within a repetitive sequence of time slots and a counter produces a series of digital addresses that are representative of a repetitive sequence of time slots to enable a comparison and generation of a latch signal at the particular time slot indicated. A probe is placed in electrical engagement with that portion of the signal corresponding to the selected digital address and a series test input signal is drawn from the system. The serial test input signal is converted from serial form to parallel form and a digital to analog converter generates a representative analog output signal that may be compared with a standardized analog signal that should be present at the desired point in the system when all components are functioning properly. Various synchronizing and clock signal rates can be provided to give the test apparatus the capability for accommodating differently sized signals for generating in different test analog signals.

Brief Summary Text - BSTX (6):

The present invention is directed to providing an apparatus for selectively monitoring a serial data stream within a repetitive sequence of time slots at a desired point in a system and for providing a representative analog output signal. A selectively variable switch provides a selected digital address signal representative of a particular time slot within the repetitive sequence of time slots and a counter circuit iteratively produces a series of digital address signals that are representative of all the repetitive sequence of time slots. A comparator circuit is coupled to receive the selected digital address signals from

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14	☐	☐	US 5295080 A	19940315	7	Method of operating a buffer memory to provide a trigger	714/
15	☐	☑	US 4751670 A	19880614	11	High integrity digital processor architecture	701/
16	☐	☑	US 4658209 A	19870414	9	Universal test board, serial input (for synthesizer	714/
17	☐	☐	US 4646303 A	19870224	20	Data error detection and	714/

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United States Patent [19]
Osborne et al.

[11] 4,001,559
[45] Jan. 4, 1977

[54] PROGRAMMABLE MEASURING

[75] Inventors: Duane C. Osborne; John M. Harrison, both of Epsom; Alfred E. Hilhman, Jr., Suncook, all of N.H.

[73] Assignee: Northern Telecom, Inc., Waltham, Mass.

[22] Filed: Dec. 16, 1974

[21] Appl. No.: 532,744

[52] U.S. Cl. ..... 235/151.31; 179/175.2 R; 340/146.1 E; 444/1

[51] Int. Cl.² G08C 25/00; G06F 15/20

[58] Field of Search ..... 235/151.3, 151.31; 340/146.1 E; 179/175.2 C, 175.21, 175.3 R, 15 AL, 175.31 R; 178/69 R, 69 A; 444/1

[56] References Cited

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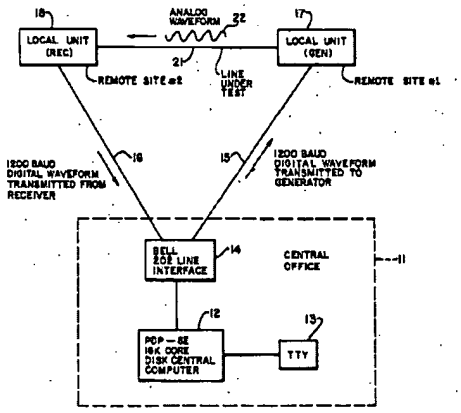
Primary Examiner—Jerry Smith
Attorney, Agent, or Firm—Charles Hieken; Jerry Cohen

[57] ABSTRACT

A communications line under test intercouples programmable local units, one of which transmits an analog waveform to the other in response to digital control signals received from a computer. The receiving programmable local unit transmits a digital signal to the computer representative of the received analog signal to thereby enable the computer to determine transmission characteristics of the communications line intercoupling the programmable local units.

13 Claims, 14 Drawing Figures



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US-PAT-NO: 4001559
DOCUMENT-IDENTIFIER: US 4001559 A
TITLE: Programmable measuring

Detailed Description Text - DETX (48):

The invention has a number of features. The concept of having one or more local programmable units communicating with a central digital computer affords great flexibility in testing at relatively low system cost reliably over relatively inexpensive communication channels to rapidly effect a wide number of tests. The local unit includes a digital input/output for communicating with a digital computer and an analog input/output for communication with a line under test. To this end it includes a shift register waveform generator that may receive a sequence of multi-bit digital numbers representative of a waveform serially at a relatively slow rate and provide these digital number signals in sequence in parallel form to a digital-to-analog converter to produce the desired test analog signal as the shift register is shifted at a much faster rate than the rate at which waveform data may enter. A similar unit may be used for accepting a digital representation of a received signal waveform and delivering it at a slower rate for transmission to the central office digital computer.

Current US Original Classification - CCOR (1):

714/714

Details | Text | Image | HTML | KWIC

19	☐	☐	US 4495623 A	19850122	24	Digital data storage in video format	714/
20	☐	☑	US 4055801 A	19771025	20	Automatic electronic test equipment and method	714/
21	☐	☑	US 4001559 A	19770104	22	Programmable measuring	714/

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